UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,767	04/03/2006	Shimura Hiroshi	29898/41747	3983

4743 7590 09/24/2010

MARSHALL, GERSTEIN & BORUN LLP
233 SOUTH WACKER DRIVE
6300 WILLIS TOWER
CHICAGO, IL 60606-6357

EXAMINER	
CHEN, QING	

ART UNIT	PAPER NUMBER
2191	

MAIL DATE	DELIVERY MODE
09/24/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,767	HIROSHI, SHIMURA	
	Examiner	**Art Unit**	
	Qing Chen	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _03 April 2006_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-14_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-14_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _21 December 2005_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _20060221, 20060629, 20061113_.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. This is the initial Office action based on the application filed on April 3, 2006.

2. **Claims 1-14** are pending.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The information disclosure statements filed on February 21, 2006, June 29, 2006, and November 13, 2006 have been considered by the Examiner. The cited documents identified as "Search Report," "Preliminary Report," and "Written Opinion" submitted by the Applicant are considered by the Examiner. However, the cited documents are official documents that are sent to the Applicant in response to examination of patent applications and cannot be listed in a printed patent publication. An initial of the Examiner will cause the cited documents to be listed in the printed patent publication and therefore, a strikethrough is applied to the cited documents.

The cited documents considered by the Examiner but will not be listed in the printed patent publication is as follows (in no particular order):

- International Search Report for PCT/JP2004/009000 dated August 31, 2004.
- International Preliminary Report on Patentability for PCT/JP2004/009000 dated May 1, 2006.
- Written Opinion for PCT/JP2004/O09000 dated May 1, 2006.
- Supplementary European Search Report for European patent application No. 04746469.8 - 2224 dated August 10, 2006.

Specification

5. The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Objections

6. **Claims 9 and 12-14** are objected to because of the following informalities:

- Claim 9 recites the limitation "a system." It should presumably read -- a *parallel processing* system --. Note that such amendment would provide sufficient antecedent basis for the limitation "the parallel processing system."
- Claims 12-14 contain a typographical error: "[I]nput in the system" should presumably read -- input *into* the system --.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. **Claims 7, 8, 13, and 14** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 7 is directed to an apparatus. However, the recited "means for" components of the apparatus appear to lack the necessary physical components (hardware) to constitute a machine

or manufacture under § 101. The recited "means for" components of the apparatus can be construed to cover software under the broadest reasonable interpretation. Therefore, the claimed apparatus is ineligible subject matter under § 101.

Claim 8 depends on Claim 7 and does not cure the deficiency of Claim 7. Therefore, Claim 8 is rejected for the same reason set forth in the rejection of Claim 7.

Claim 13 is directed to a simulator. However, the recited components of the simulator appear to lack the necessary physical components (hardware) to constitute a machine or manufacture under § 101. The recited components of the simulator can be construed to cover software under the broadest reasonable interpretation. Therefore, the claimed simulator is ineligible subject matter under § 101.

Claim 14 is directed to a program product. However, the program product does not define any structural and functional interrelationships between the program product and any hardware elements of a computer, which permit the program product's functionality to be realized. While on the contrary, a man-made tangible embodiment storing the program product would permit the program product's functionality to be realized. Therefore, the claimed program product is ineligible subject matter under § 101.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2003/0154466 (hereinafter "Snider") in view of US 2004/0088685 (hereinafter "Poznanovic").

As per Claim 1, Snider discloses:

A method for forming (page 5, "A method of compiling …")**, in accordance with a definition file** (paragraph [0025], "The source code 102 …")**, a parallel processing system that includes a plurality of types of elements that operate in parallel** (paragraph [0038], "In step 310, the mid-level optimization process 300, determines which computations are on the critical path. The critical path can be a plurality of computations being carried out in parallel [parallel processing system]."; paragraph [0053], "The process 300 generates a plurality of configuration instruction sets representing a plurality of hardware realizations (design spaces) [plurality of types of elements].")**,**

the definition file including a plurality of parallel descriptions that respectively define a plurality of parallel processes performed independently (paragraph [0025], "The source code 102 [definition file] typically includes of programming statements [plurality of parallel descriptions] …"; paragraph [0038], "In step 310, the mid-level optimization process 300, determines which computations are on the critical path. The critical path can be a plurality of computations being carried out in parallel [plurality of parallel processes].")**, the plurality of parallel descriptions including a first parallel description showing a first parallel process**

with a plurality of data inputs including at least one data input into which output data of another parallel process is inputted (paragraph [0038], "… a loop may have one computation of C=A*B [first parallel process with a plurality of data inputs] followed by and another computation A=C+D [at least one data input into which output data of another parallel process is inputted]. Both the multiplication and addition operations are on the critical path")**,**

and the method comprising:

a first step of generating, based on a hardware library in which information on the plurality of types of elements is stored, hardware configuration information including circuit configurations for executing the parallel processes defined by the parallel descriptions of the definition file (Figures 4A-4D; paragraph [0044], "In step 340, the output of steps 310-330, may include a plurality of configuration instruction sets [hardware library], wherein each instruction set is operable to <u>generate</u> a different optimized hardware realization [circuit configuration] (emphasis added)."; paragraph [0054], "FIGS. 4(A-D) illustrates a plurality of hardware realizations that can be implemented from the above software. Each of the plurality of realizations has specific area, speed and power characteristics.")**, the circuit configurations including at least one of the plurality of types of elements** (Figures 4A-4D; paragraph [0055], "FIG. 4A illustrates an unpipelined multiplier circuit 400 [at least one of the plurality of types of elements] which can be implemented by optimization process. The unpipelined multiplier circuit 400 operates by receiving inputs via operands, a and b every clock cycle (II=1) and produces one result (c) at the end of the clock cycle.")**.**

Snider does not explicitly disclose:

- **a second step of adding a delay element to the hardware configuration information so that data with a same latency from input into the parallel processing system are inputted into a plurality of data inputs of a circuit configuration for executing the first parallel process.**

However, Poznanovic discloses:

- **a second step of adding a delay element to hardware configuration information so that data with a same latency from input into a parallel processing system are inputted into a plurality of data inputs of a circuit configuration for executing a first parallel process** (Figure 27; paragraph [0170], "The dataflow graph may expose <u>instruction-level parallelism</u> (emphasis added)."; paragraph [0236], "FIG. 27, at left, shows a DFG fragment [hardware configuration information] that computes the expression C=A-(A+B)*B [first parallel process] … Because of the node latencies, the values appearing at the ports of the multiply and subtract nodes may not aligned properly. Delay nodes [delay elements], which are fixed length FIFO queues, may be inserted [added] as shown at right. The insertion is done such that, for every node in the DFG, the path lengths to all of its inputs may be equal [data with a same latency].")**.**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Poznanovic into the teaching of Snider to include a second step of adding a delay element to the hardware configuration information so that data with a same latency from input into the parallel processing system are inputted into a plurality of data inputs of a circuit configuration for executing the first parallel process. The modification would be obvious because one of ordinary skill in the art would be motivated to adjust the latencies for the unaligned input data of the circuit nodes so that the latencies for all of

the input data of the circuit nodes are equal in a parallel processing system (Poznanovic, paragraph [0236]).

As per Claim 2, the rejection of Claim 1 is incorporated; and Snider further discloses:

- **wherein the parallel processing system is reconfigurable to different hardware configurations by changing connections between the plurality of types of elements** (paragraph [0027], "A configuration instruction set (which is a netlist for a custom circuit or configuration instructions for an FPGA) is output from the hardware complier 106 for reconfiguring FPGA 104 in order to generate the desired circuit.") **and the hardware configuration information includes information showing a plurality of different hardware configurations** (Figures 4A-4D; paragraph [0054], "FIGS. 4(A-D) illustrates a plurality of hardware realizations [plurality of different hardware configurations] that can be implemented from the above software. Each of the plurality of realizations has specific area, speed and power characteristics.")**.**

As per Claim 3, the rejection of Claim 1 is incorporated; and Snider further discloses:

- **wherein the plurality of types of elements include a plurality of types of operation units of a scale whereby one operation unit is capable of processing parallel process defined by one parallel description of the definition file** (Figures 4A-4D; paragraph [0055], "FIG. 4A illustrates an unpipelined multiplier circuit 400 [plurality of types of operation units of a scale] which can be implemented by optimization process. The unpipelined multiplier

circuit 400 operates by receiving inputs via operands, a and b every clock cycle (II=1) and produces one result (c) at the end of the clock cycle [parallel process].”)**.**

As per Claim 4, the rejection of Claim 1 is incorporated; and Snider does not explicitly disclose:

- **wherein the plurality of types of elements include a plurality of types of operation units for executing different operations in byte or word units.**

However, Poznanovic discloses:

- **wherein a plurality of types of elements include a plurality of types of operation units for executing different operations in byte or word units** (paragraph [0302], “The FPGA bitstream files are read into a buffer as 4096 byte quantities. This buffer is then packed into 64-bit words and written out to the bitstream array contained in the appropriate bitstream's structure.”)**.**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Poznanovic into the teaching of Snider to include wherein the plurality of types of elements include a plurality of types of operation units for executing different operations in byte or word units. The modification would be obvious because one of ordinary skill in the art would be motivated to process data in byte quantities to be used in FPGA bitstream files (Poznanovic, paragraph [0302]).

As per Claim 5, the rejection of Claim 1 is incorporated; and Snider does not explicitly disclose:

- **wherein information on a number of cycles consumed by respective types of elements is stored in the hardware library, and**

- **in the second step, the delay element corresponding to a number of cycles consumed by at least one of the plurality of types of elements is added.**

However, Poznanovic discloses:

- **wherein information on a number of cycles consumed by respective types of elements is stored in a hardware library** (paragraph [0127], "A hardware logic module information file entry is delimited with a begin-def and end-def marker, and takes the form: …"; paragraph [0130], "LATENCY=<num>; The <num> is an integer value specifying the number of clock cycles between the presentation of data to the hardware logic module's inputs and the availability of corresponding results on the outputs.")**, and**

- **a delay element corresponding to a number of cycles consumed by at least one of a plurality of types of elements is added** (Figure 27; paragraph [0236], "FIG. 27, at left, shows a DFG fragment that computes the expression C=A-(A+B)*B, with some assumed latencies [corresponding to a number of cycles consumed by at least one of a plurality of types of elements] next to the nodes … Because of the node latencies, the values appearing at the ports of the multiply and subtract nodes may not aligned properly. Delay nodes [delay elements], which are fixed length FIFO queues, may be inserted [added] as shown at right. The insertion is done such that, for every node in the DFG, the path lengths to all of its inputs may be equal [data with a same latency]."). *[Examiner's Remarks: Note that Figure 27 clearly illustrates the delay nodes added with the corresponding number of cycles consumed by the circuit nodes to adjust the latency differences.]*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Poznanovic into the teaching of Snider to include wherein information on a number of cycles consumed by respective types of elements is stored in the hardware library, and in the second step, the delay element corresponding to a number of cycles consumed by at least one of the plurality of types of elements is added. The modification would be obvious because one of ordinary skill in the art would be motivated to adjust the latencies for the unaligned input data of the circuit nodes so that the latencies for all of the input data of the circuit nodes are equal in a parallel processing system (Poznanovic, paragraph [0236]).

As per Claim 6, the rejection of Claim 1 is incorporated; and Snider further discloses:

- **wherein the plurality of parallel descriptions include a second parallel description that defines a second parallel process including shared processing that is common** (paragraph [0038], "In step 310, the mid-level optimization process 300, determines which computations are on the critical path. The critical path can be a plurality of computations being carried out in parallel … a loop may have one computation of C=A*B followed by and another computation A=C+D [second parallel process including shared processing that is common]. Both the multiplication and addition operations are on the critical path")**.**

Snider does not explicitly disclose:

- **a third parallel process defined by a third parallel description,**
- **in the first step, a shared circuit configuration including at least one of the plurality of types of elements is generated for the shared processing, and**

- **in the second step, the delay element is added to a circuit configuration for executing a difference between the second parallel process and the shared processing as the circuit configuration for executing the first parallel process.**

However, Poznanovic discloses:

- **a third parallel process defined by a third parallel description** (Figure 27; paragraph [0170], "The dataflow graph may expose instruction-level parallelism (emphasis added)."; paragraph [0236], "FIG. 27, at left, shows a DFG fragment [hardware configuration information] that computes the expression C=A-(A+B)*B [third parallel process] …"),

- **a shared circuit configuration including at least one of a plurality of types of elements is generated for shared processing** (Figure 27), *[Examiner's Remarks: Note that Figure 27 clearly illustrates that the addition node calculates the sum for input data "A" and "B" which is shared with the multiplication node.]* **and**

- **a delay element is added to a circuit configuration for executing a difference between a second parallel process and the shared processing as the circuit configuration for executing a first parallel process** (Figure 27; paragraph [0170], "The dataflow graph may expose instruction-level parallelism (emphasis added)."; paragraph [0236], "FIG. 27, at left, shows a DFG fragment [hardware configuration information] that computes the expression C=A-(A+B)*B [first parallel process] … Because of the node latencies, the values appearing at the ports of the multiply and subtract nodes may not aligned properly [difference between second parallel process and shared processing]. Delay nodes [delay elements], which are fixed length FIFO queues, may be inserted [added] as shown at right. The insertion is done such that, for every node in the DFG, the path lengths to all of its inputs may be equal.").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Poznanovic into the teaching of Snider to include a third parallel process defined by a third parallel description, in the first step, a shared circuit configuration including at least one of the plurality of types of elements is generated for the shared processing, and in the second step, the delay element is added to a circuit configuration for executing a difference between the second parallel process and the shared processing as the circuit configuration for executing the first parallel process. The modification would be obvious because one of ordinary skill in the art would be motivated to adjust the latencies for the unaligned input data of the circuit nodes so that the latencies for all of the input data of the circuit nodes are equal in a parallel processing system (Poznanovic, paragraph [0236]).

Claims 7 and 8 are apparatus claims corresponding to the method claims above (Claims 1 and 2) and, therefore, are rejected for the same reasons set forth in the rejections of Claims 1 and 2.

Claim 9 is a program product claim corresponding to the method claim above (Claim 1) and, therefore, is rejected for the same reason set forth in the rejection of Claim 1.

As per Claim 10, Snider discloses:

A computer-readable recording medium (paragraph [0024], "… a memory device 110.") **on which a definition file** (paragraph [0025], "The source code 102 …") **is stored, the definition file including a plurality of parallel descriptions that respectively define a**

plurality of parallel processes performed independently and in synchronization by a system that includes a plurality of elements that operate in parallel, (paragraph [0025], "The source code 102 [definition file] typically includes of programming statements [plurality of parallel descriptions] …"; paragraph [0038], "In step 310, the mid-level optimization process 300, determines which computations are on the critical path. The critical path can be a plurality of computations being carried out in parallel [plurality of parallel processes performed independently and in synchronization]."; paragraph [0053], "The process 300 generates a plurality of configuration instruction sets representing a plurality of hardware realizations (design spaces) [plurality of elements]."**), the plurality of parallel descriptions including a first parallel description showing a first parallel process with a plurality of data inputs including at least one data input into which output data of another parallel process is inputted** (paragraph [0038], "… a loop may have one computation of C=A*B [first parallel process with a plurality of data inputs] followed by and another computation A=C+D [at least one data input into which output data of another parallel process is inputted]. Both the multiplication and addition operations are on the critical path")**.**

Snider does not explicitly disclose:

- **showing that data with a same latency from input into the system are inputted into the plurality of data inputs.**

However, Poznanovic discloses:

- **showing that data with a same latency from input into a system are inputted into a plurality of data inputs** (Figure 27; paragraph [0236], "FIG. 27, at left, shows a DFG fragment that computes the expression C=A-(A+B)*B [plurality of data inputs] … Because of

the node latencies, the values appearing at the ports of the multiply and subtract nodes may not aligned properly. Delay nodes, which are fixed length FIFO queues, may be inserted as shown at right. The insertion is done such that, for every node in the DFG, the path lengths to all of its inputs may be equal [data with a same latency].”).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Poznanovic into the teaching of Snider to include showing that data with a same latency from input into the system are inputted into the plurality of data inputs. The modification would be obvious because one of ordinary skill in the art would be motivated to adjust the latencies for the unaligned input data of the circuit nodes so that the latencies for all of the input data of the circuit nodes are equal in a parallel processing system (Poznanovic, paragraph [0236]).

As per Claim 11, the rejection of Claim 10 is incorporated; and Snider does not explicitly disclose:

- **wherein the plurality of parallel descriptions respectively define a plurality of parallel processes to be executed in synchronization with a clock for operations by the plurality of elements.**

However, Poznanovic discloses:

- **wherein a plurality of parallel descriptions respectively define a plurality of parallel processes to be executed in synchronization with a clock for operations by a plurality of elements** (Figure 27; paragraph [0170], “The dataflow graph may expose <u>instruction-level parallelism</u> (emphasis added).”; paragraph [0236], “FIG. 27, at left, shows a

DFG fragment that computes the expression C=A-(A+B)*B [plurality of parallel processes], with some assumed latencies next to the nodes. Below it is a chart showing the values of the signals on each clock tick. Because of the node latencies, the values appearing at the ports of the multiply and subtract nodes [plurality of elements] may not aligned properly. Delay nodes, which are fixed length FIFO queues, may be inserted as shown at right. The insertion is done such that, for every node in the DFG, the path lengths to all of its inputs may be equal."; paragraph [0339], "Clock-accurate simulation assumes the existence of a system clock, and the functional units execute synchronously, coordinated by the clock.")**.**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Poznanovic into the teaching of Snider to include wherein the plurality of parallel descriptions respectively define a plurality of parallel processes to be executed in synchronization with a clock for operations by the plurality of elements. The modification would be obvious because one of ordinary skill in the art would be motivated to calculate the clock cycles needed in order to adjust the latencies for the unaligned input data of the circuit nodes so that the latencies for all of the input data of the circuit nodes are equal in a parallel processing system (Poznanovic, paragraph [0236]).

As per Claim 12, Snider discloses:

A method of simulating (paragraph [0046], "The simulator is used to test the hardware … as shown in step 350.")**, based on a definition file** (paragraph [0025], "The source code 102 …")**, a system that includes a plurality of types of elements that operate in parallel** (paragraph [0038], "In step 310, the mid-level optimization process 300, determines which

computations are on the critical path. The critical path can be a plurality of computations being carried out in parallel [parallel processing system]."; paragraph [0053], "The process 300 generates a plurality of configuration instruction sets representing a plurality of hardware realizations (design spaces) [plurality of types of elements]."**),**

the definition file including a plurality of parallel descriptions that respectively define a plurality of parallel processes performed independently (paragraph [0025], "The source code 102 [definition file] typically includes of programming statements [plurality of parallel descriptions] …"; paragraph [0038], "In step 310, the mid-level optimization process 300, determines which computations are on the critical path. The critical path can be a plurality of computations being carried out in parallel [plurality of parallel processes]."**), the plurality of parallel descriptions including a first parallel description showing a first parallel process with a plurality of data inputs including at least one data input into which output data of another parallel process is inputted** (paragraph [0038], "… a loop may have one computation of C=A*B [first parallel process with a plurality of data inputs] followed by and another computation A=C+D [at least one data input into which output data of another parallel process is inputted]. Both the multiplication and addition operations are on the critical path"**).**

Snider does not explicitly disclose:

- **the method comprising a step of executing a plurality of parallel processes defined by the definition file in synchronization, wherein in the step of executing, data with a same latency from input in the system are inputted into the plurality of data inputs of the first parallel process.**

However, Poznanovic discloses:

- **a step of executing a plurality of parallel processes defined by a definition file in synchronization, wherein in the step of executing, data with a same latency from input into a system are inputted into a plurality of data inputs of a first parallel process** (Figure 27; paragraph [0054], "… an HLL source code file 102 [definition file] …"; paragraph [0170], "The dataflow graph may expose <u>instruction-level parallelism</u> (emphasis added)."; paragraph [0236], "FIG. 27, at left, shows a DFG fragment that computes the expression C=A-(A+B)*B [plurality of data inputs of a first parallel process] … Because of the node latencies, the values appearing at the ports of the multiply and subtract nodes may not aligned properly. Delay nodes, which are fixed length FIFO queues, may be inserted as shown at right. The insertion is done such that, for every node in the DFG, the path lengths to all of its inputs may be equal [data with a same latency]."; paragraph [0339], "Clock-accurate simulation assumes the existence of a system clock, and the functional units execute synchronously, coordinated by the clock.")**.**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Poznanovic into the teaching of Snider to include the method comprising a step of executing a plurality of parallel processes defined by the definition file in synchronization, wherein in the step of executing, data with a same latency from input in the system are inputted into the plurality of data inputs of the first parallel process. The modification would be obvious because one of ordinary skill in the art would be motivated to adjust the latencies for the unaligned input data of the circuit nodes so that the latencies for all of the input data of the circuit nodes are equal in a parallel processing system (Poznanovic, paragraph [0236]).

Claim 13 is a simulator claim corresponding to the method claim above (Claim 12) and, therefore, is rejected for the same reason set forth in the rejection of Claim 12.

Claim 14 is a program product claim corresponding to the method claim above (Claim 12) and, therefore, is rejected for the same reason set forth in the rejection of Claim 12.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Qing Chen whose telephone number is 571-270-1071. The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 4:00 PM. The Examiner can also be reached on alternate Fridays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wei Zhen, can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Q. C./

Examiner, Art Unit 2191

/Anna Deng/

Primary Examiner, Art Unit 2191